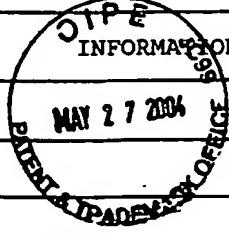


U.S. Department of Commerce, Patent and Trademark Office	Serial Number: 10/690,874
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	Inventor: Anatoliy V. Tsyrganovich
	Group Art Unit: <del>2017</del> 2816
Frequency Locked Loop	Examiner name: <del>Unknown</del> HAI L. NGUYEN
	Attorney Docket No. ZIL-521-1P

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*Examiner Initial		Number	Date	Applicants	Class	Subclass	Filing Date, If Appropriate
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		Document Number	Priority Date	Country	Applicant	Pub. Date	Yes	No

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	D	T. Olsson and Peter Nilsson, "An all-Digital PLL Clock Multiplier," Dept of Electrosience, Lund Univerity, Lund, Sweden, date unknown (perhaps 2002), downloaded on 5/24/2004 from <a href="http://www.ap-asic.org/2002/proceedings/5B/5B-3.PDF">http://www.ap-asic.org/2002/proceedings/5B/5B-3.PDF</a> , 4 pages.
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↓	F	D. Abramovitch, "Lyapunov Redesign of Classical Digital Phase-Lock Loops," Agilent Labs, Palo Alto, CA, dated June 5, 2003, downloaded on 5/24/2004 from <a href="http://www.labs.agilent.com/personal/Danny%20Abramovitch/pubs/lpll%20cdig%20talk.pdf">http://www.labs.agilent.com/personal/Danny Abramovitch/pubs/lpll cdig talk.pdf</a> , 22 pages.

Examiner: HAI L. NGUYEN

Date Considered

04/24/2005

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.